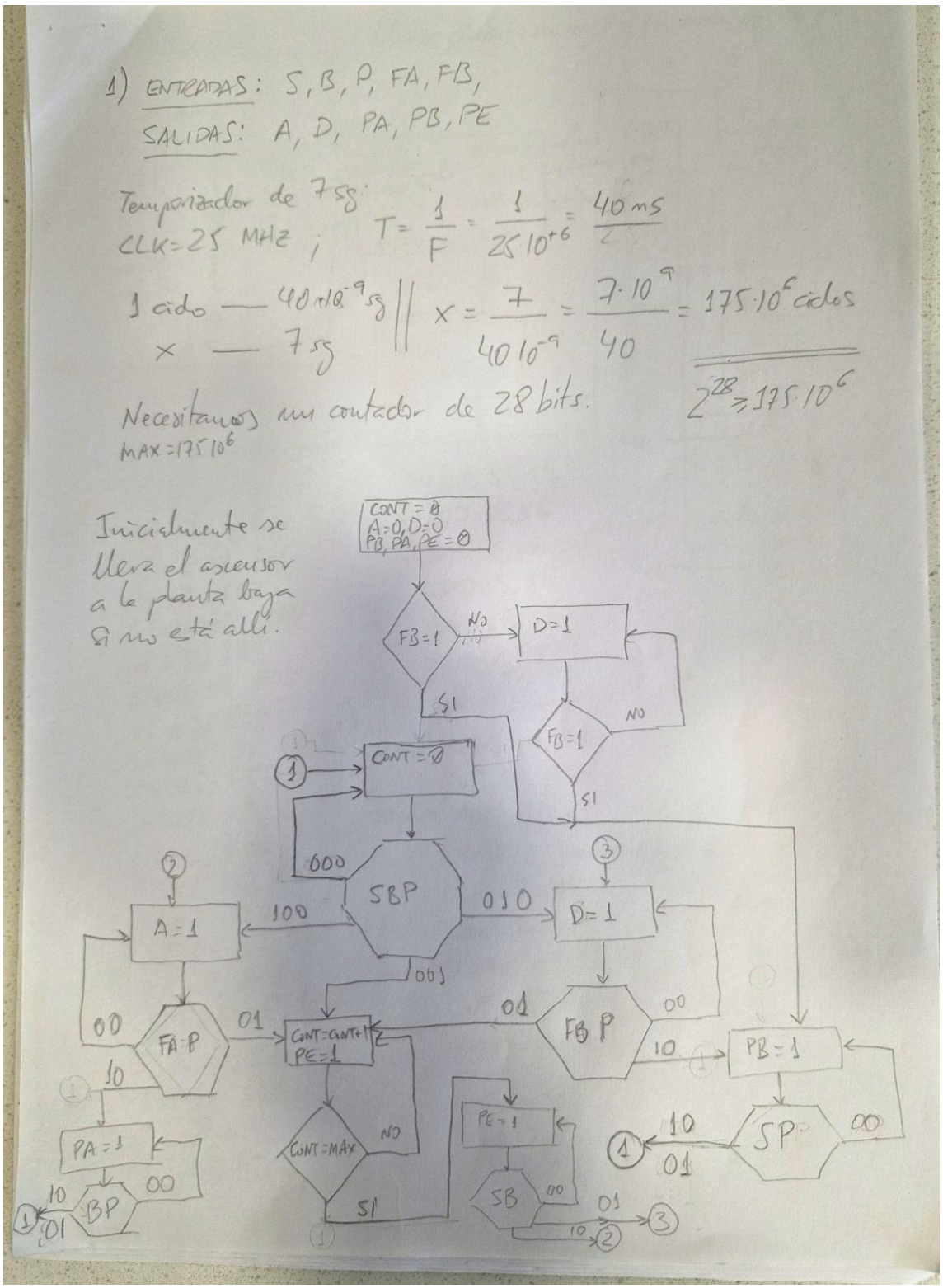
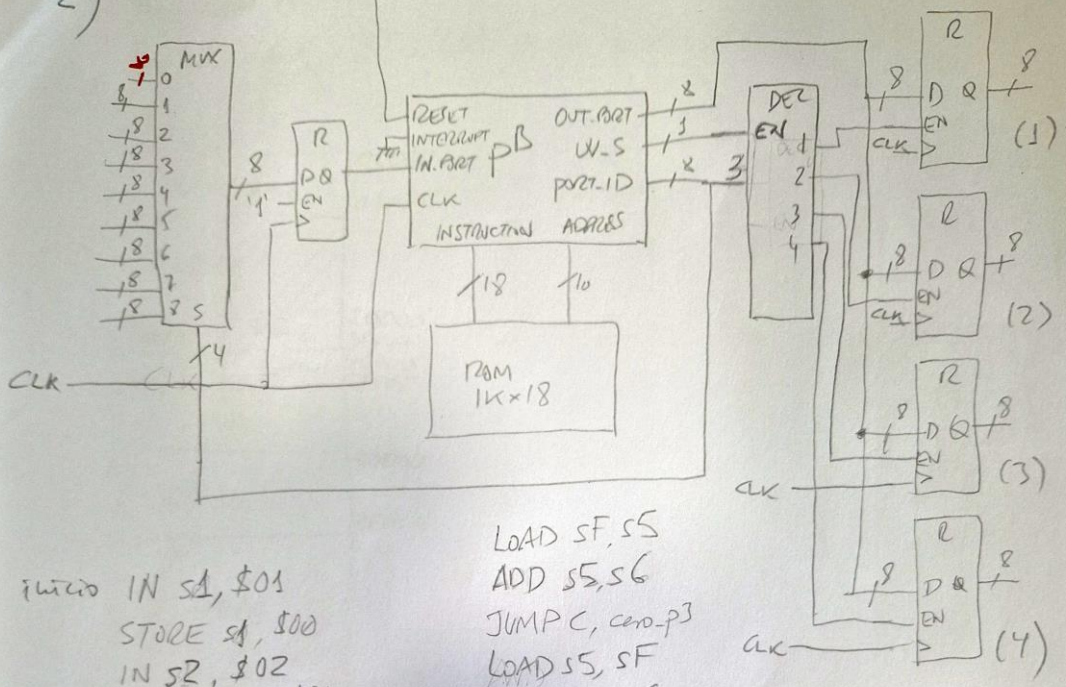
SOLUCIÓN DEL EXAMEN DE JUNIO 2025 (SISTEMAS DIGITALES II)



2)

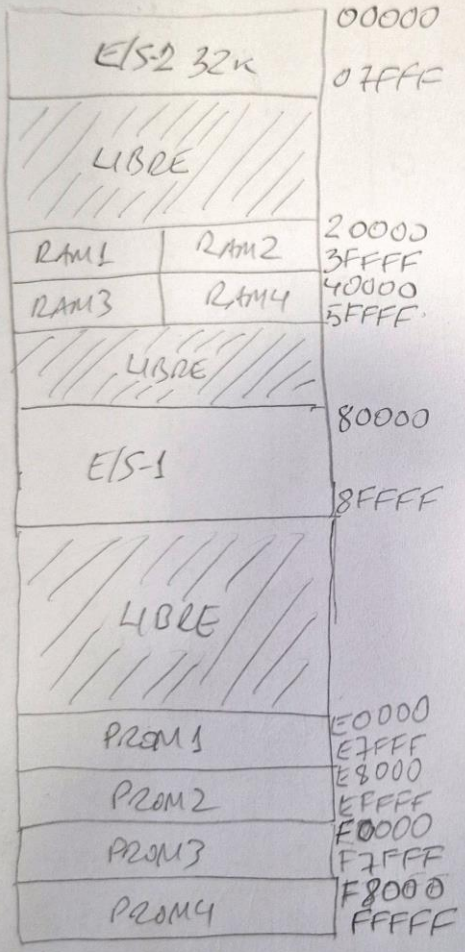
(Puede colocarse un registro en cada canal del MUX)



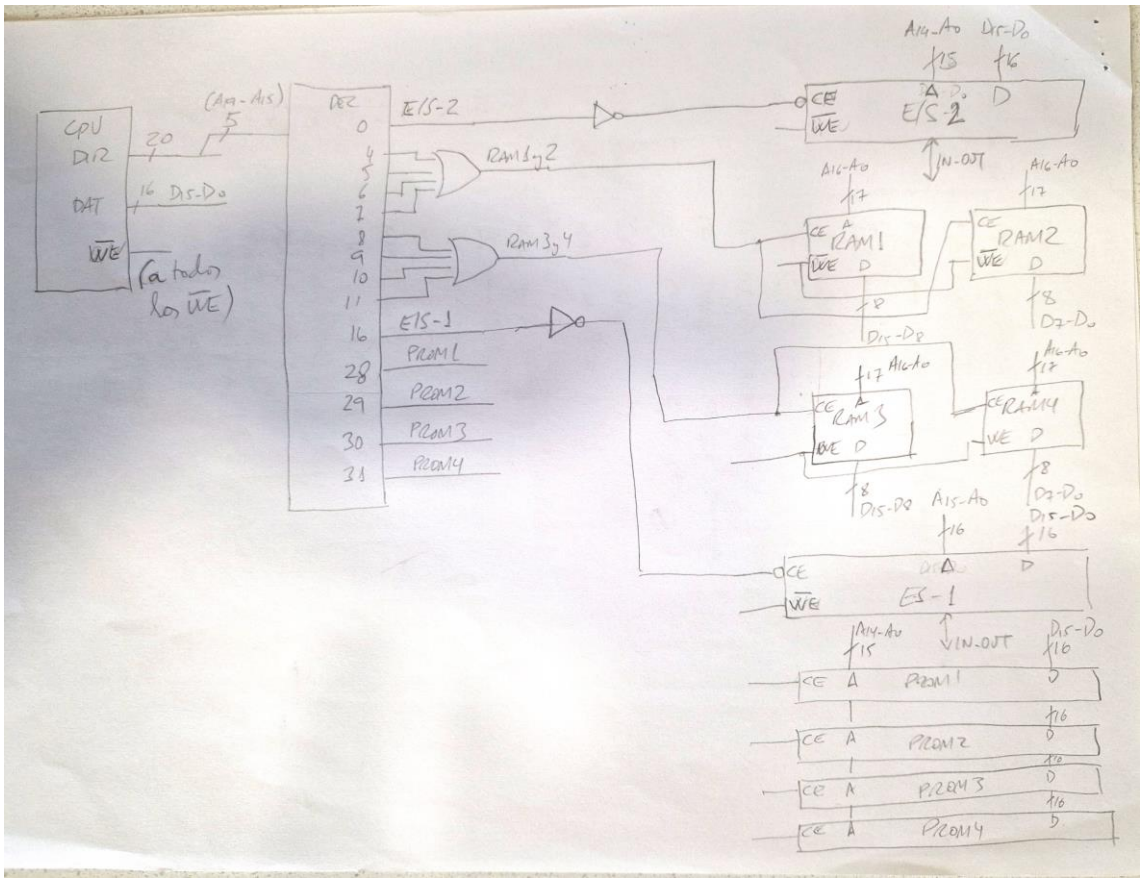

```
inicio  IN s1, $01
        STORE s1, $00
        IN s2, $02
        STORE s2, $01
        IN s3, $03
        STORE s3, $02
        IN s4, $04
        STORE s4, $03
        IN s5, $05
        STORE s5, $04
        IN s6, $06
        STORE s6, $05
        IN s7, $07
        STORE s7, $06
        IN s8, $08
        STORE s8, $07
        SUB s1, s2
        OUT s1, $01
        OR s8, s4
        OUT s3, $02
        LOAD sF, s5
        ADD s5, s6
        JUMP C, cero_p3
        LOAD s5, sF
        AND s5, s6
        OUT s5, $03
        JUMP seguir
cero_p3 LOAD sA, $00
        OUT sA, $03
seguir  XOR s7, s8
        JUMP Z, poner_a_1
        OUT s7, $04
        JUMP inicio
poner_a_1 LOAD sB, 0xFF
        OUT sB, $04
        JUMP inicio
```

3) Bus datos: 16 bits

Bus direcciones: $2^n = 1M \Rightarrow n = 20$ bits



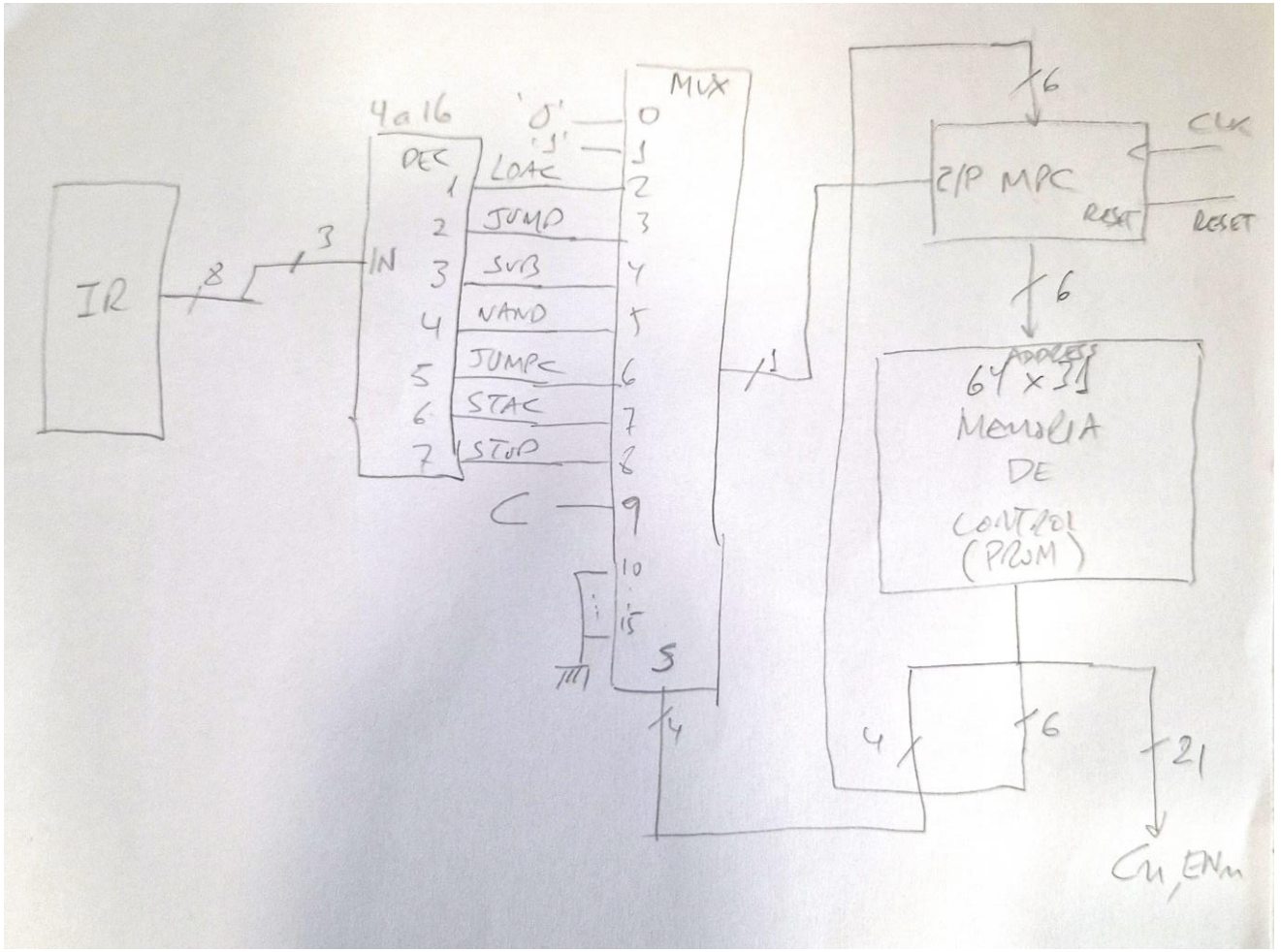
MÓDULO	HEX	A19 A18 A17 A16 A15	A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	SAL. DEC.
E/S-2	00000 07FFF	0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0
RAM1 y 2	20000 3FFFF	0 0 1 0 0 0 0 1 1 1	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	4,5,6,7
RAM3 y 4	40000 5FFFF	0 1 0 0 0 0 1 0 1 1	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	8,9,10,11
E/S-1	80000 8FFFF	1 0 0 0 0 1 0 0 0 1	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	16
PROM 1	E0000 E7FFF	1 1 1 0 0 1 1 1 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	28
PROM 2	E8000 EFFFF	1 1 1 0 1 1 1 1 0 1	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	29
PROM 3	F0000 F7FFF	1 1 1 1 0 1 1 1 1 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	30
PROM 4	F8000 FFFFF	1 1 1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	31



4)

```
0          PC ← 0
1  carga   MARH ← PCH
2          MARL ← PCL
3          MDR ← M[MAR], PC ← PC+1
4          IR ← MDR
5          IF LDAC THEN ldac
6          IF SUB THEN sub
7          IF NAND THEN naud
8          IF JUMP C THEN jumpc
9          IF STAC THEN stac
10 stop    GOTO stop
11 ldac    MARH ← PCH
12         MARL ← PCL
13         MDR ← M[MAR], PC ← PC+1
14         AC ← MDR
15         GOTO carga
16 sub     MARH ← PCH
17         MARL ← PCL
18         MDR ← M[MAR], PC ← PC+1
19         RT ← MDR
20         MARH ← PCH
21         MARL ← PCL
22         MDR ← M[MAR], PC ← PC+1
23         MARL ← MDR
24         MARH ← RT
25         MDR ← M[MAR]
26         AC ← AC - MDR
27         GOTO carga
28 naud    MARH ← PCH
29         MARL ← PCL
30         MDR ← M[MAR], PC ← PC+1
31         AC ← AC AND MDR
```

```
32          AC ← not AC
33          GOTO carga
34 jumpc    IF C=1 THEN saltar
35          PC ← PC+1
36          PC ← PC+1
37          GOTO carga
38 saltar   MARH ← PCH
39          MARL ← PCL
40          MDR ← M[MAR], PC ← PC+1
41          RT ← MDR
42          MARH ← PCH
43          MARL ← PCL
44          MDR ← M[MAR], PC
45          PCH ← RT
46          PCL ← MDR
47          GOTO carga
48 jump     GOTO saltar
49 stac     MARH ← PCH
50          MARL ← PCL
51          MDR ← M[MAR], PC ← PC+1
52          RT ← MDR
53          MARH ← PCH
54          MARL ← PCL
55          MDR ← M[MAR], PC ← PC+1
56          MARL ← MDR
57          MARH ← RT
58          MDR ← AC
59          M[MAR] ← MDR
60          GOTO carga
```


IR
8
3
4a16
DEC
IN
1
2
3
4
5
6
7
LOAC
JUMP
SUB
NAND
JUMPC
STAC
STOP
C
'0'
'1'
MUX
0
1
2
3
4
5
6
7
8
9
10
15
5
4
6
21
C4, ENm
C/P MPC
CLK
RESET
6
64 x 31
ADDRESS
MEMORIA
DE
CONTROL
(PROM)